Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An improved method for detecting errors in configuration data frames loaded into a frame register of a Programmable Logic Device (PLD) and reloading only erroneous configuration data frames comprising the steps of:

clearing the frame register of a configuration memory of the PLD;

loading a new configuration data frame into the frame register and into an error detection circuit;

checking said data frame for errors and transferring data in the frame register to memory cells of the PLD if no error is detected;

reloading the frame register of the PLD and incrementing an error counter value if errors are encountered; and

repeating above steps until all desired configuration data frames are loaded.

2. (Currently Amended) The method as claimed in claim 1, further comprising the step of aborting the loading and reloading if the error counter value equals a ~~pre-determined~~ threshold value.

3. (Original) The method as claimed in claim 1 wherein the error checking is performed using an error detection algorithm including cyclic redundancy checking and parity checking.

4. (Original) The method as claimed in claim 1 wherein the error counter value is reset before loading a new configuration data frame in the frame register.

5. (Original) The method as claimed in claim 1 wherein reloading of the frame is achieved by adjusting an address counter when the PLD operates as a Master.

6. (Original) The method as claimed in claim 1 wherein reloading of the frame is achieved by signaling an external controller to adjust an address counter when the PLD operates as a Slave.

7. (Original) The method of claim 1 further comprising operating the PLD as a master.

8. (Original) The method of claim 1 further comprising operating the PLD as a slave.

9. (Currently Amended) An improved Programmable Logic Device (PLD) incorporating a circuit arrangement for detecting errors in configuration data frames loaded into its frame register and reloading erroneous configuration data frames, comprising:

error detecting means for checking the configuration data loaded in the frame register,

error counting means for incrementing an error count for each error detected in said configuration data frame,

comparing means for comparing the error count to a ~~pre-determined~~ threshold value, and

reloading means for reloading a configuration data frame into the frame register if errors are encountered.

10. (Currently Amended) The improved PLD as claimed in claim 9, further comprising means for aborting a PLD configuration process in case the error counter value equals the ~~pre-determined~~ threshold value.

11. (Original) The improved PLD as claimed in claim 9 wherein the error detecting means implements an error detection algorithm including cyclic redundancy checking and parity checking.

12. (Original) The improved PLD as claimed in claim 9 wherein a controller is provided to reset the error count before loading a new configuration data frame in the frame register.

13. (Original) The improved PLD as claimed in claim 9 wherein the reloading means comprises an address counter to enable reloading of the erroneous frame into the frame register in case of errors when the PLD operates as a Master.

14. (Original) The improved PLD as claimed in claim 9 wherein the reloading means comprises an external controller to enable reloading of the erroneous frame into the frame register in case of errors when the PLD operates as a Slave.

15. (Original) The improved PLD as claimed in claim 9 wherein the PLD is configured as a master.

16. (Original) The improved PLD as claimed in claim 9 wherein the PLD is configured as a slave.

17. (Currently Amended) A method of configuring a programmable logic device (PLD), comprising:

loading a first one of a plurality of configuration data frames into a frame register;

checking the loaded data frame for errors;

if an error is detected, repeating the above steps for the configuration data frame in which an error was detected; ~~and~~

if an error is not detected, transferring data from the frame register to at least one memory ~~cell.~~ cell; and

subsequently repeating the above steps for a second configuration data frame in the plurality of configuration data frames.

18. (Canceled)

19. (Original) The method of claim 17 wherein the step of checking the loaded data frame for errors comprises running a cyclic redundancy check.

20. (Original) The method of claim 17, further comprising incrementing an error count when an error is detected.

21. (Currently Amended) The method of claim 20, further comprising aborting the configuration if the error count exceeds a ~~preset~~ threshold number.

22. (Original) The method of claim 20, further comprising resetting the error count when data is transferred from the frame register to the at least one memory cell.

23. (Original) The method of claim 17 wherein the PLD comprises a field programmable gate array.

24. (Original) The method of claim 17, further comprising configuring the PLD as a master.

25. (Original) The method of claim 17, further comprising configuring the PLD as a slave.

26. (Original) The method of claim 17, further comprising identifying the one of a plurality of configuration data frames using an address counter.

27. (Original) The method of claim 17, further comprising clearing the frame register.

28. (Original) The method of claim 17 wherein the at least one memory cell comprises a latch.

29. (Currently Amended) A system for configuring a programmable logic device (PLD), comprising:

means for sequentially loading a plurality of configuration data frames;

means for detecting errors in a loaded configuration data frame;

means for correcting detected errors in a loaded configuration data frame without reloading other configuration data frames and before loading subsequent configuration data frames; and

means for storing data contained in the plurality of configuration data frames.

30. (Original) The system of claim 29, further comprising means for aborting configuration.

31. (Original) The system of claim 29 wherein the means for loading a configuration data frame, the means for detecting errors, the means for correcting errors and the means for storing data are part of a PLD.

32. (Original) A programmable logic device (PLD), comprising:

a configuration frame register to load a plurality of configuration data frames;

a plurality of memory cells to store configuration data; and

an error detection circuit to detect errors in a loaded configuration data frame, wherein the PLD is configured to reload a single configuration data frame into the configuration frame register upon detecting an error and to transfer data from the configuration frame register to at least one of the plurality of memory cells in the absence of an error.

33. (New) The programmable logic device of claim 32 wherein the error detection circuit comprises an error counter and the PLD is configured to abort loading of a configuration data frame if an error count equals a threshold value.

34. (New) The programmable logic device of claim 33 wherein the error counter is reset before loading a new configuration data frame in the frame register.

35. (New) The programmable logic device of claim 32 wherein the PLD is configured to reload the frame by adjusting an address counter when the PLD operates as a Master.

36. (New) The programmable logic device of claim 32 wherein the PLD is configured to reload the frame by signaling an external controller to adjust an address counter when the PLD operates as a Slave.